

## **REMARKS**

### **I. Introduction**

Claims 16 to 135 are currently pending in the present application.

The Examiner requires restriction to one of the following inventions:

- I: Claims 16 to 74 and 107 to 120 directed to an instruction pipeline that couples an array with a standard processor; and
- II: Claims 75 to 106 and 121 to 135 directed to a cache memory including IRAM memory elements and storing local cache copies of a main memory.

Accordingly, *Applicants elect, without traverse, Group II, which corresponds to claims 75 to 106 and 121 to 135.*

Applicants respectfully request an early and favorable action on the merits.

Respectfully submitted,

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